

### FEATURES

- Complete angular rate digital gyroscope**
- 14-bit resolution**
- Scalable measurement range**
- Initial range:  $\pm 80^\circ/\text{sec}$  (typical)**
- Increase range with external resistor**
- Z-axis (yaw rate) response**
- SPI digital output interface**
- High vibration rejection over wide frequency**
- 2000 g-powered shock survivability**
- 1 KHz bandwidth**
- Selectable using external capacitor**
- Externally controlled self-test**
- Internal temperature sensor output**
- Dual auxiliary 14-bit ADC inputs**
- Absolute rate output for precision applications**
- 5 V single-supply operation**
- 8.2 mm  $\times$  8.2 mm  $\times$  5.2 mm package**
- 40°C to +105°C operation**
- RoHS compliant**

### APPLICATIONS

- Platform stabilization
- Image stabilization
- Guidance and control
- Inertia measurement units
- Robotics

### GENERAL DESCRIPTION

The ADIS16060 is a yaw-rate gyroscope with an integrated serial peripheral interface (SPI). It features an externally selectable bandwidth response and scalable dynamic range.

The SPI port provides access to the rate sensor, an internal temperature sensor, and two external analog signals (using internal ADC). The digital data available at the SPI port is proportional to the angular rate about the axis that is normal to the top surface of the package.

An additional output pin provides a precision voltage reference. Two digital self-test inputs electromechanically excite the sensor to test the operation of the sensor and the signal-conditioning circuits.

The ADIS16060 is available in an 8.2 mm  $\times$  8.2 mm  $\times$  5.2 mm, 16-terminal, peripheral land grid array (LGA) package.

### FUNCTIONAL BLOCK DIAGRAM

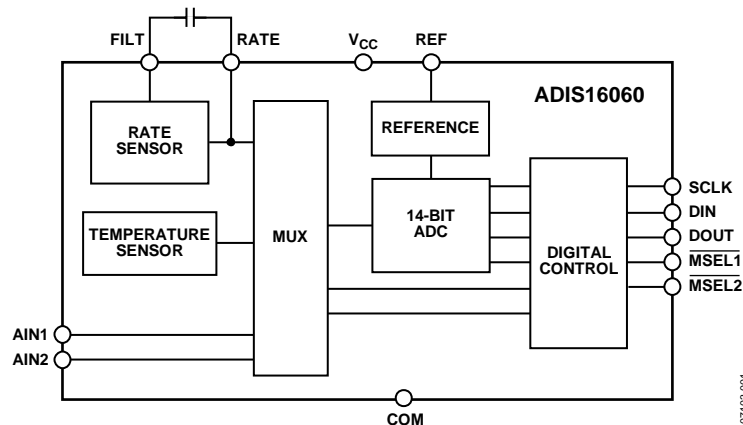


Figure 1.

#### Rev. PrB

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## SPECIFICATIONS

$T_A = 25^\circ\text{C}$ ,  $V_{CC} = V_{DRIVE} = 5\text{ V}$ , angular rate =  $0^\circ/\text{sec}$ ,  $C_{OUT} = 0\ \mu\text{F}$ ,  $\pm 1\text{ g}$ , unless otherwise noted.

Table 1.

Parameter	Conditions	Min <sup>1</sup>	Typ	Max <sup>1</sup>	Unit
<b>SENSITIVITY</b>					
Dynamic Range <sup>2</sup>	Full-scale range over specifications range	$\pm 50$	$\pm 80$		$^\circ/\text{sec}$
Initial	Clockwise rotation is positive output, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	0.01168	0.0121	0.01296	$^\circ/\text{sec}/\text{LSB}$
Change Over Temperature <sup>3</sup>	$V_{CC} = V_{DRIVE} = 4.75\text{ V}$ to $5.25\text{ V}$		$\pm 2$		%
Nonlinearity	Best fit straight line		0.1		$^\circ/\text{sec}$
<b>NULL</b>					
Initial	Nominal $0^\circ/\text{sec}$ output is 2048 LSB	-44		+44	$^\circ/\text{sec}$
Change Over Temperature <sup>3</sup>	$V_{CC} = V_{DRIVE} = 4.75\text{ V}$ to $5.25\text{ V}$	-0.53	$\pm 0.11$	+0.53	$^\circ/\text{sec}/^\circ\text{C}$
Turn-On Time	Power on to $\pm 0.5^\circ/\text{sec}$ of final value		10		ms
Linear Acceleration Effect	Any axis		0.1		$^\circ/\text{sec}/\text{g}$
Voltage Sensitivity	$V_{CC} = V_{DRIVE} = 4.75\text{ V}$ to $5.25\text{ V}$		$\pm 1$		$^\circ/\text{sec}/\text{V}$
<b>NOISE PERFORMANCE</b>					
Total Noise	0.1 Hz to 1 kHz		2		$^\circ/\text{sec}$ rms
Rate Noise Density	@ $25^\circ\text{C}$		0.04		$^\circ/\text{sec}/\sqrt{\text{Hz}}$
<b>FREQUENCY RESPONSE</b>					
3 dB Bandwidth (User-Selectable) <sup>4</sup>	$C_{OUT} = 0\ \mu\text{F}$	1		1000	Hz
Sensor Resonant Frequency			14.5		kHz
<b>SELF-TEST INPUTS</b>					
ST POS <sup>5</sup>	ST1 pin from Logic 0 to Logic 1				LSB
ST NEG <sup>5</sup>	ST2 pin from Logic 0 to Logic 1				LSB
<b>TEMPERATURE SENSOR</b>					
Reading at 298 K		7700	8192	8684	LSB
Scale Factor	Proportional to absolute temperature		0.0342		K/LSB
<b>2.5 V REFERENCE</b>					
Voltage Value		2.45	2.5	2.55	V
Load Drive to Ground	Source		100		$\mu\text{A}$
Load Regulation	$0\ \mu\text{A} < I_{OUT} < 100\ \mu\text{A}$		5.0		mV/mA
Power Supply Rejection	$V_{CC} = V_{DRIVE} = 4.75\text{ V}$ to $5.25\text{ V}$		1.0		mV/V
Temperature Drift	Delta from $25^\circ\text{C}$		5.0		mV
<b>LOGIC INPUTS</b>					
Input High Voltage, $V_{INH}$		2.4			V
Input Low Voltage, $V_{INL}$				0.8	V
Input Current, $I_{IN}$	Typically 10 nA	-1		+1	$\mu\text{A}$
Input Capacitance, $C_{IN}$			5		pF
Input Capacitance, $C_{IN}$ (SCLK)			8		pF
<b>ANALOG INPUTS</b>					
Resolution	For $V_{IN} < V_{CC}$		14		Bits
Integral Nonlinearity		-6		+6	LSB
Differential Nonlinearity	No missing codes to 15 <sup>th</sup> bit	0		+2	LSB
Offset Error, $T_{MIN}$ to $T_{MAX}$		-1.6		+1.6	mV
Offset Error Temp Drift			$\pm 0.3$		ppm/ $^\circ\text{C}$
Gain Error, $T_{MIN}$ to $T_{MAX}$		-24		+24	LSB
Gain Error Temp Drift			$\pm 0.3$		ppm/ $^\circ\text{C}$
Input Voltage Range		0		$V_{REF} \times 2$	V
Leakage Current			1		nA
Input Capacitance			3		pF
Full Power Bandwidth			100		kHz

Parameter	Conditions	Min <sup>1</sup>	Typ	Max <sup>1</sup>	Unit
DIGITAL OUTPUTS					
Output High Voltage (V <sub>OH</sub> )	I <sub>SOURCE</sub> = 500 μA	V <sub>DRIVE</sub> - 0.2			V
Output Low Voltage (V <sub>OL</sub> )	I <sub>SINK</sub> = 500 μA			0.4	V
CONVERSION RATE					
Conversion Time	16 SCLK cycles with SCLK at 20 MHz			10	μs
Throughput Rate				100	kSPS
POWER SUPPLY	All at T <sub>A</sub> = -40°C to +85°C				
V <sub>CC</sub>		4.75	5	5.25	V
V <sub>CC</sub> Quiescent Supply Current	V <sub>CC</sub> @ 5 V, f <sub>SCLK</sub> = 50 kSPS		2.6	5.1	mA
Power Dissipation	V <sub>CC</sub> and V <sub>DRIVE</sub> @ 5 V, f <sub>SCLK</sub> = 50 kSPS		13	26	mW
TEMPERATURE RANGE	Operation	-40		+105	°C

<sup>1</sup> All minimum and maximum specifications are guaranteed. Typical specifications are neither tested nor guaranteed.

<sup>2</sup> Dynamic range is the maximum full-scale measurement range possible, including output swing range, initial offset, sensitivity, offset drift, and sensitivity drift at 5 V supply.

<sup>3</sup> Defined as the output change from ambient to maximum temperature, or ambient to minimum temperature.

<sup>4</sup> Frequency at which the response is 3 dB down from dc response. Bandwidth =  $1/(2 \times \pi \times 180 \text{ k}\Omega \times (22 \text{ nF} + C_{OUT}))$ . For C<sub>OUT</sub> = 0, bandwidth = 40 Hz. For C<sub>OUT</sub> = 1 μF, bandwidth = 0.87 Hz.

<sup>5</sup> Self-test response varies with temperature.

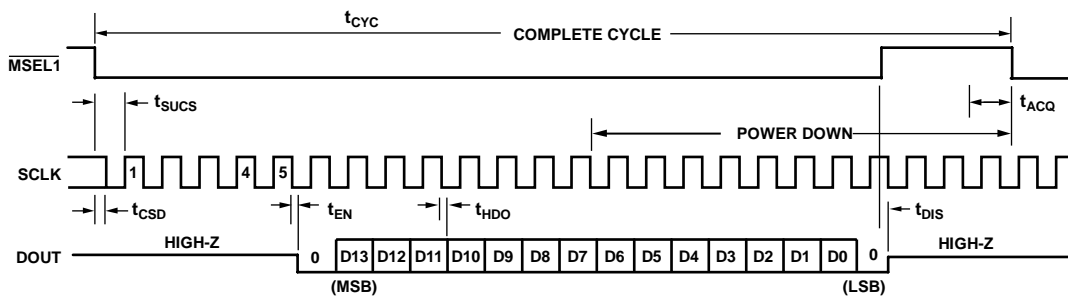
**TIMING SPECIFICATIONS**

T<sub>A</sub> = 25°C, angular rate = 0°/sec, unless otherwise noted.<sup>6</sup>

**Table 2. Read/Output Sequence**

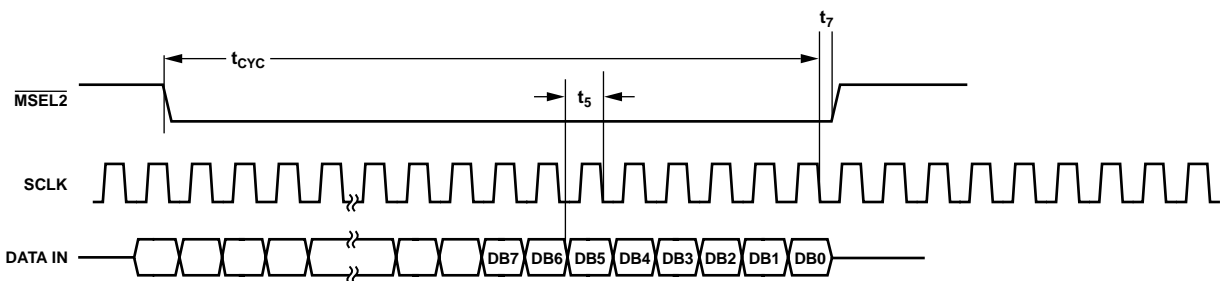
Parameter	Figure Reference	Symbol	Min	Typ	Max	Unit
Throughput Rate	See Figure 2	t <sub>CYC</sub>			100	kHz
$\overline{CS}$ Falling to DCLOCK Low	See Figure 2	t <sub>CSD</sub>			0	μs
$\overline{CS}$ Falling to DCLOCK Rising	See Figure 2	t <sub>SUCS</sub>	20			ns
DCLOCK Falling to Data Remains Valid	See Figure 2	t <sub>HDO</sub>	5	16		ns
$\overline{CS}$ Rising Edge to D <sub>OUT</sub> High Impedance	See Figure 2	t <sub>DIS</sub>		14	100	ns
DCLOCK Falling to Data Valid	See Figure 2	t <sub>EN</sub>		16	50	ns
Acquisition Time	See Figure 2	t <sub>ACQ</sub>	400			ns
D <sub>OUT</sub> Fall Time	See Figure 2	t <sub>F</sub>		11	25	ns
D <sub>OUT</sub> Rise Time	See Figure 2	t <sub>R</sub>		11	25	ns
Data Setup Time	See Figure 3	t <sub>5</sub>		5		ns
SCLK Falling Edge to MSEL2 Rising Edge	See Figure 3	t <sub>7</sub>		0		ns

<sup>6</sup> Guaranteed by design. All input signals are specified with t<sub>tr</sub> and t<sub>fr</sub> = 5 ns (10% to 90% of V<sub>CC</sub>) and timed from a voltage level of 1.6 V. The 5 V operating range spans from 4.75 V to 5.25 V.



NOTE:  
A MINIMUM OF 20 CLOCK CYCLES ARE REQUIRED FOR 14-BIT CONVERSION. SHOWN ARE 24 CLOCK CYCLES.  
DOUT GOES LOW ON THE DCLOCK FALLING EDGE FOLLOWING THE LSB READING.

Figure 2. Serial Interface Timing Diagram—Read/Output Sequence (CPOL = 0, CPHA = 0)



NOTE:  
THE LAST EIGHT BITS CLOCKED IN ARE LATCHED WITH THE RISING EDGE OF THE  $\overline{MSEL2}$  LINE.

Figure 3. Serial interface Timing—Input/Configuration Sequence (CPOL = 0, CPHA = 1)

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration (Any Axis, Unpowered, 0.5 ms)	2000 <i>g</i>
Acceleration (Any Axis, Powered, 0.5 ms)	2000 <i>g</i>
V <sub>CC</sub> to COM	-0.3 V to +6.0 V
V <sub>DRIVE</sub> to COM	-0.3 V to V <sub>CC</sub> + 0.3 V
Analog Input Voltage to COM	-0.3 V to V <sub>CC</sub> + 0.3 V
Digital Input Voltage to COM	-0.3 V to +7.0 V
Digital Output Voltage to COM	-0.3 V to V <sub>CC</sub> + 0.3 V
ST1/ST2 Input Voltage to COM	-0.3 V to V <sub>CC</sub> + 0.3 V
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

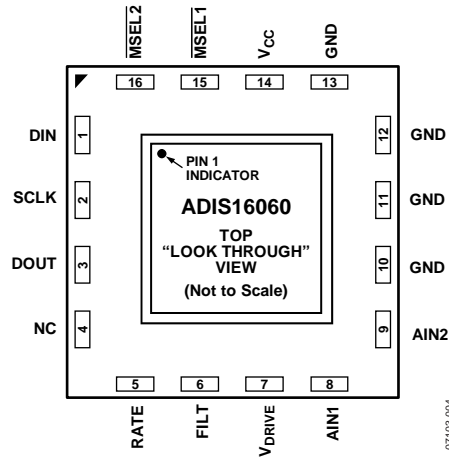
Drops onto hard surfaces can cause shocks of greater than 2000 *g* and exceed the absolute maximum rating of the device. Care should be exercised in handling to avoid damage.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



**NOTES**

1. NC = NO CONNECT
2. THIS IS NOT AN ACTUAL "TOP VIEW," AS THE PINS ARE NOT VISIBLE FROM THE TOP. THIS IS A LAYOUT VIEW, WHICH REPRESENTS THE PIN CONFIGURATION, IF THE PACKAGE IS LOOKED THROUGH FROM THE TOP. THIS CONFIGURATION IS PROVIDED FOR PCB LAYOUT PURPOSES.

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type <sup>1</sup>	Description
1	DIN	I	SPI Data Input.
2	SCLK	I	SPI Serial Clock.
3	DOUT	O	SPI Data Output.
4	NC		No Connect.
5	RATE	O	Buffered Analog Output. Represents the angular rate signal.
6	FILT	I	External Capacitor Connection to Control Bandwidth.
7	V <sub>DRIVE</sub>	S	SPI Power Supply. This can be the receive processing circuit's supply to simplify interfacing.
8	AIN1	I	External Analog Input Channel 1.
9	AIN2	I	External Analog Input Channel 2.
10	GND	S	Ground.
11	GND	O	Ground.
12	GND	I	Ground.
13	GND	I	Ground.
14	V <sub>CC</sub>	S	Analog Power.
15	MSEL1	I	SPI, Mode Select 1. Used for data output functions.
16	MSEL2	I	SPI, Mode Select 2. Used for data input functions.

<sup>1</sup> I = input; O = output; S = power supply.

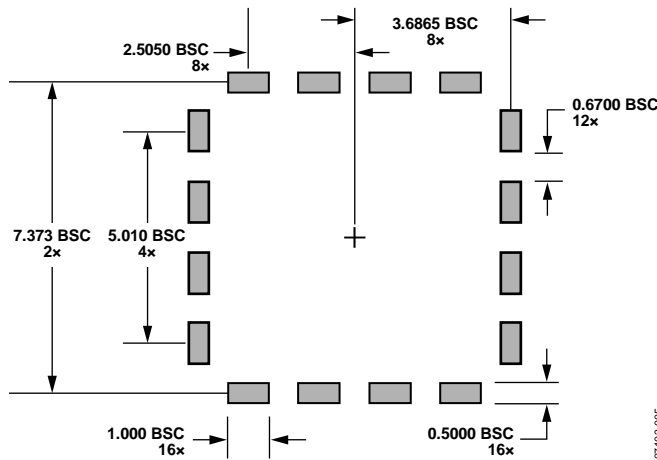


Figure 5. Second-Level Assembly Pad Layout

TYPICAL PERFORMANCE CHARACTERISTICS

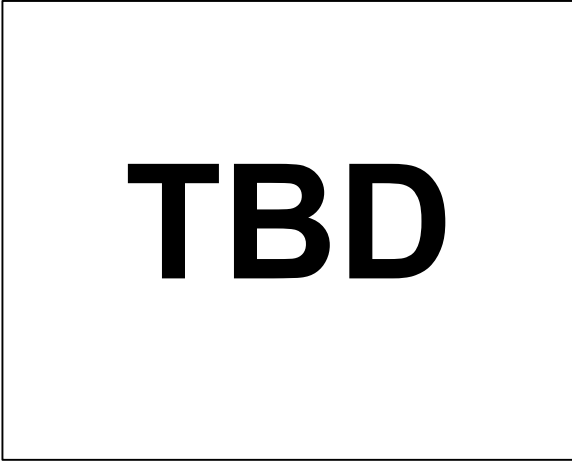


Figure 6.

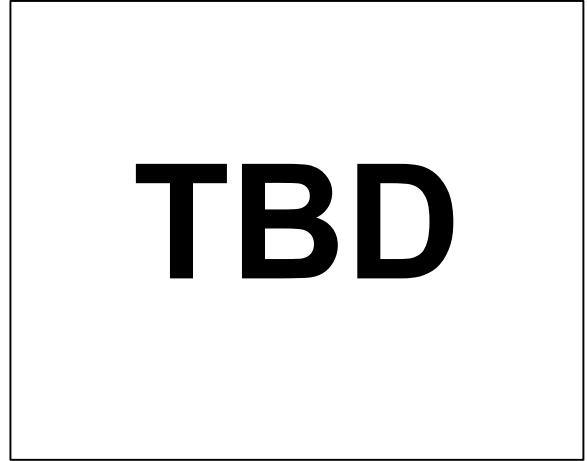


Figure 9.

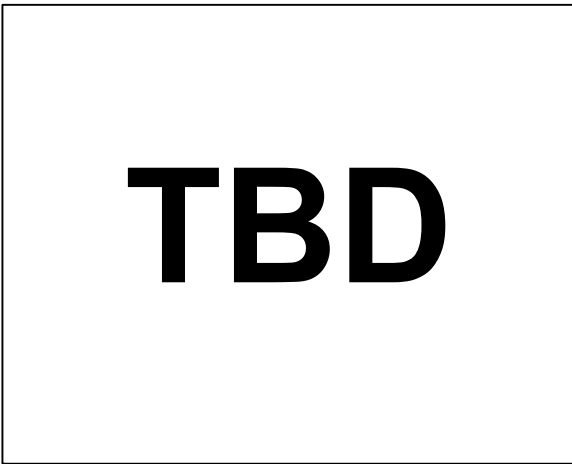


Figure 7.

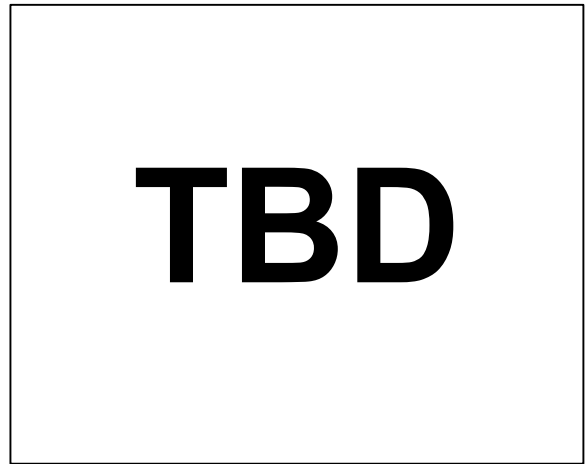


Figure 10.

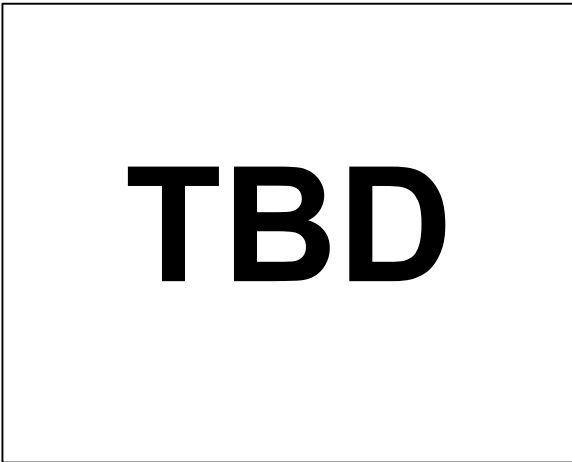


Figure 8.

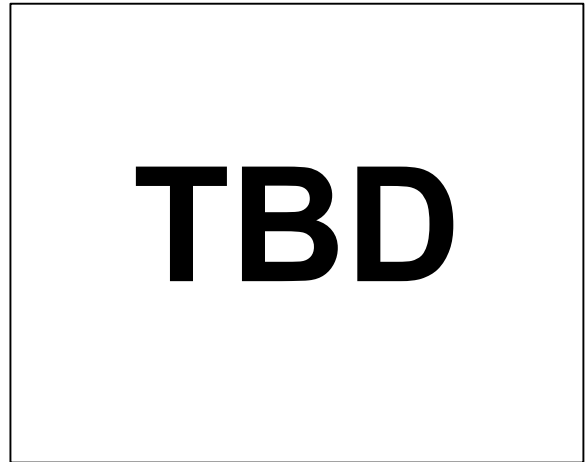
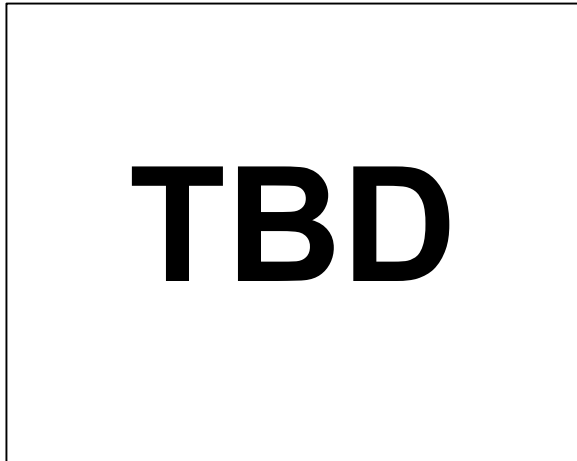
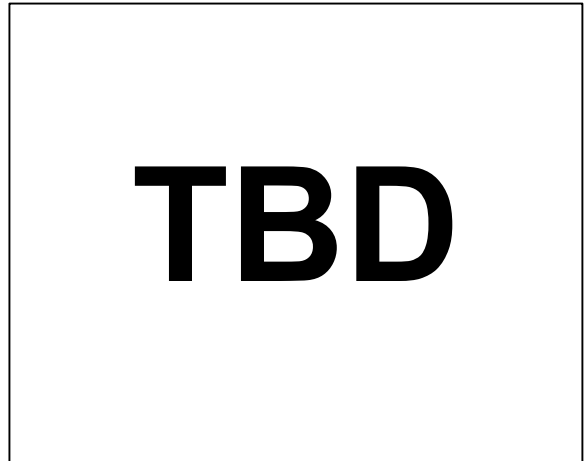


Figure 11.

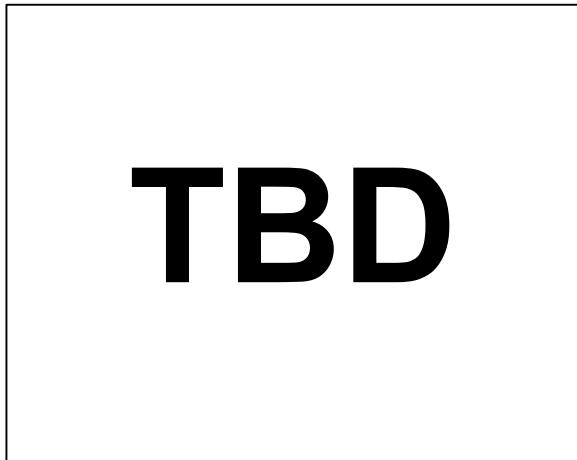




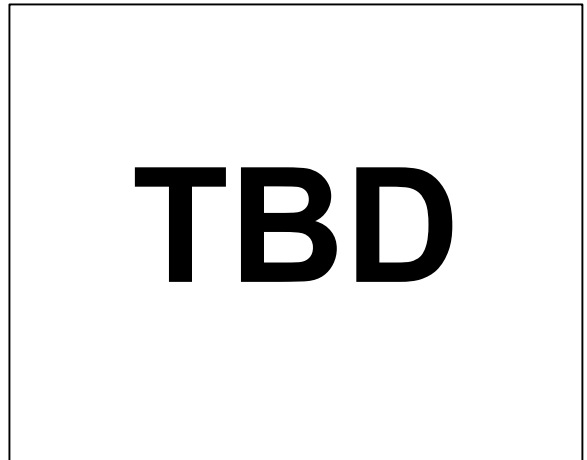
*Figure 12.*



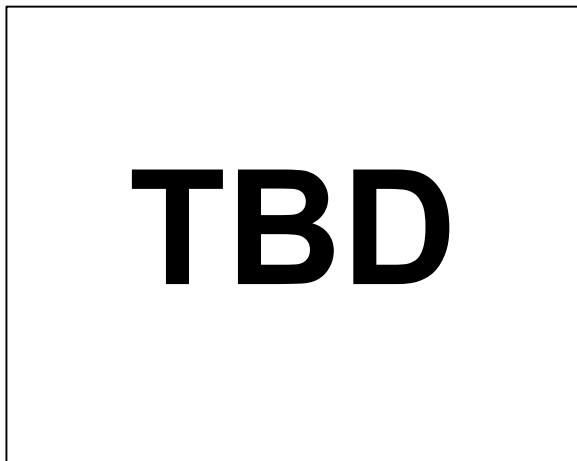
*Figure 15.*



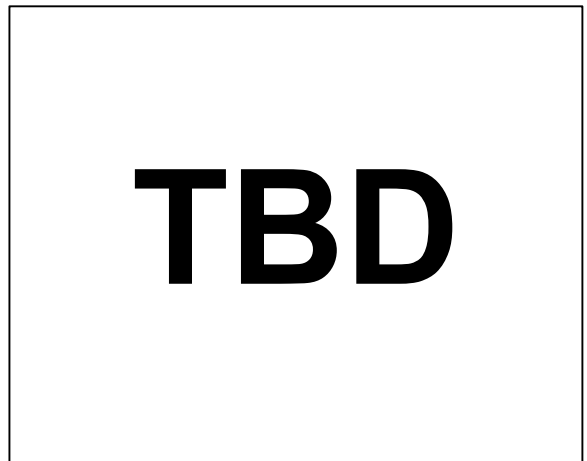
*Figure 13.*



*Figure 16.*



*Figure 14.*



*Figure 17.*

## THEORY OF OPERATION

The ADIS16060 operates on the principle of a resonator gyroscope. Two polysilicon sensing structures each contain a dither frame that is electrostatically driven to resonance. This produces the necessary velocity element to produce a Coriolis force while rotating. At two of the outer extremes of each frame, orthogonal to the dither motion, are movable fingers that are placed between fixed pickoff fingers to form a capacitive pickoff structure that senses Coriolis motion. The resulting signal is fed to a series of gain and demodulation stages that produce the electrical rate signal output. The rate signal is then converted to a digital representation of the output on the SPI pins. The dual-sensor design rejects external  $g$  forces and vibration. Fabricating the sensor with the signal conditioning electronics preserves signal integrity in noisy environments.

The electrostatic resonator requires 14 V to 16 V for operation. Because only 5 V is typically available in most applications, a charge pump is included on-chip. After the demodulation stage, there is a single-pole, low-pass filter included on-chip that is used to limit high frequency artifacts before final amplification. The frequency response is dominated by the second low-pass filter, which is set by adding capacitance across RATE and FILT.

### RATE SENSITIVE AXIS

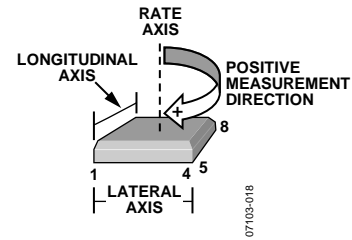


Figure 18. Rate Signal Increases with Clockwise Rotation

## BASIC OPERATION

The ADIS16060 is designed for simple integration into industrial system designs, requiring only a 5.0 V power supply, two mode select lines and three serial communications lines. The SPI handles all digital I/O communication in the ADIS16060.

### SERIAL PERIPHERAL INTERFACE (SPI)

The ADIS16060 SPI port includes five signals: master select 1 (MSEL1), master select 2 (MSEL2), serial clock (SCLK), data input (DIN), and data output (DOUT). The MSEL1 line is used when reading data out of the sensor (DOUT) and the MSEL2 line is used when configuring the sensor (DIN).

#### Selecting Output Data

Refer to Table 5 to determine the appropriate DIN bit sequence based on the required data source. Table 2 and Figure 3 provide the necessary timing details for the input configuration sequence. Once the MSEL2 goes high, the last eight, DIN bits are loaded into the internal control register, which represents DB0-DB7 in Table 5.

### Output Data Access

Use Table 2 and Figure 2 to determine the appropriate timing considerations for reading output data.

### OUTPUT DATA FORMATTING

All of the output data is in an offset-binary format, which in this case, means that the ideal output for a zero rate condition is 8192 codes. If the sensitivity is equal to 0.0121°/s/LSB, then a rate of +10°/s results in a change of 826 codes, and a digital rate output of +9018 codes. If an offset error of -20°/s is introduced, this reduces the output by 1653 codes (typical sensitivity assumed), resulting in a digital rate output of 7365 codes.

### ADC CONVERSION

The internal, successive approximation ADC begins the conversion process on the falling edge of MSEL1 and begins to place data, MSB-first, on the DOUT line, on the 6<sup>th</sup> falling edge of SCLK, as shown in Figure 2. The entire conversion process takes 22 SCLK cycles. Once MSEL1 goes high, the acquisition process starts, in preparation for the next conversion cycle.

Table 5. DIN Configuration Bit Assignments

Action	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Measure Angular Rate (Gyro)	0	0	1	0	0	0	0	0
Measure Temperature	0	0	0	1	0	0	0	0
Measure AIN2	1	0	0	0	0	0	0	0
Measure AIN1	0	1	0	0	0	0	0	0
Set Positive Self-Test	X	X	X	X	0	0	0	1
Set Negative Self-Test	X	X	X	X	0	0	1	0

## APPLICATIONS INFORMATION

### SUPPLY AND COMMON CONSIDERATIONS

Power supply noise and transient behaviors can influence the accuracy and stability of any sensor-based measurement system. When considering the power supply for the ADIS16060, it is important to understand that the ADIS16060 provides 0.2 μF of decoupling capacitance on the V<sub>CC</sub> pin. Depending on the level of noise present in the system power supply, the ADIS16060 may not require any additional decoupling capacitance for this supply. The analog supply, V<sub>CC</sub>, and the digital drive supply, V<sub>DRIVE</sub>, are segmented to allow multiple logic levels to be used in receiving the digital output data. V<sub>DRIVE</sub> is intended for the down-stream logic power supply and supports standard 3.3 V and 5 V logic families. The V<sub>DRIVE</sub> supply does not have internal decoupling capacitors.

### SETTING BANDWIDTH

External Capacitor C<sub>OUT</sub> is used in combination with the on-chip R<sub>OUT</sub> resistor to create a low-pass filter to limit the bandwidth of the ADIS16060 rate response. The -3 dB frequency set by R<sub>OUT</sub> and C<sub>OUT</sub> is:

$$f_{OUT} = \frac{1}{2 \times \pi \times R_{OUT} \times C_{OUT}}$$

and can be well controlled because R<sub>OUT</sub> has been trimmed during manufacturing to be 200 kΩ ±1%. Setting the range with an external resistor will impact R<sub>OUT</sub> as follows:

$$R_{OUT} = \frac{(200 \text{ k}\Omega \times R_{EXT})}{(200 \text{ k}\Omega + R_{EXT})}$$

In general, an additional hardware or software filter is added to attenuate high frequency noise arising from demodulation spikes at the gyro's 14 kHz resonant frequency (the noise spikes at 14 kHz can be clearly seen in the power spectral density curve shown in Figure 19).

### INCREASING MEASUREMENT RANGE

Scaling the measurement range requires the addition of a single resistor, connected across the RATE and FILT pins. The following relationship provides proper relationship for selecting the appropriate resistor:

$$R_{EXT} = \frac{200 \text{ k}\Omega}{\Delta - 1}, \quad \Delta = \text{Increase in range}$$

Table 6. Standard Resistor Values, Resulting Range

R <sub>EXT</sub>	°/sec	R <sub>EXT</sub>	°/sec	R <sub>EXT</sub>	°/sec
806k	100	133k	200	49.9k	401
402k	120	100k	240	43.2k	450
267k	140	80.6k	279	38.3k	498
200k	160	66.5k	321	34.0k	551
158k	181	56.2k	365	30.9k	598

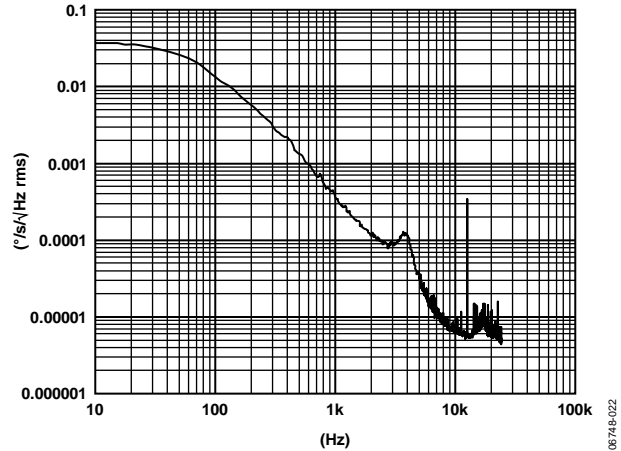


Figure 19. Noise Spectral Density with 2-Pole, Low-Pass Filter (40 Hz and 250 Hz)

### DYNAMIC DIGITAL SENSITIVITY SCALING

This device supports in-system, dynamic, digital sensitivity scaling. At this printing, an application note (AN-942) is being drafted to provide further details.

### TEMPERATURE MEASUREMENTS

When using the temperature sensor, an acquisition time of greater than 40 μs helps to ensure proper setting and measurement accuracy. See Table 2 and Figure 2 for details on the definition of acquisition time.

### SELF-TEST FUNCTION

Exercising the self-test function is simple as shown in this example.

1. Configure using DIN = 00100001 (Positive self-test, rate selected).
2. Read output.
3. Configure using DIN = 00100000 (Positive self-test off, rate selected)
4. Read output.
5. Calculate the difference between Step 2 and Step 4, and compare this with the specified self-test output changes in the Specifications section.

Exercising the negative self-test requires changing the sequence in Step 1 to DIN = 00100010.

### OUTLINE DIMENSIONS

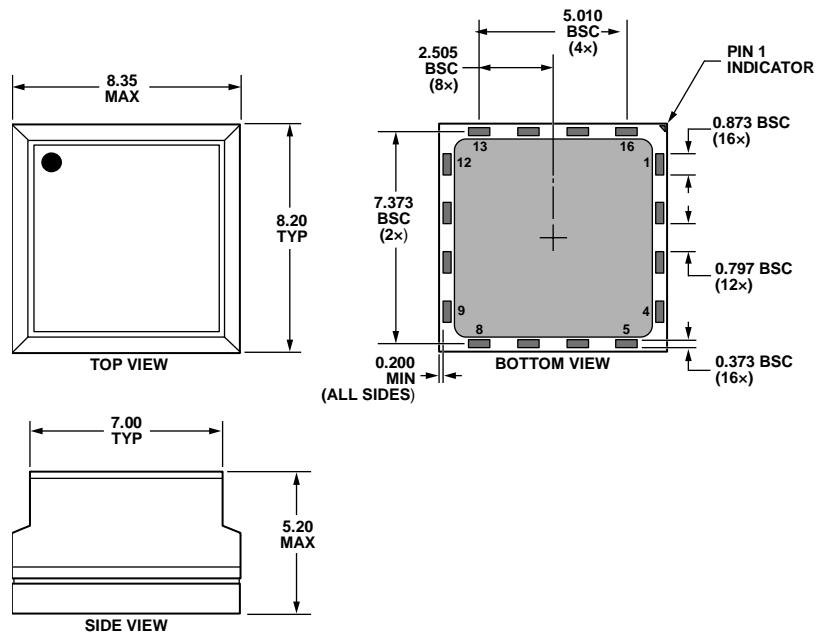


Figure 20. 16-Terminal Stacked Land Grid Array [LGA]  
(CC-16-1)  
Dimensions shown in millimeters

002107-B

### ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADIS16060BCCZ <sup>1</sup>	-40°C to +105°C	16-Terminal Stacked Land Grid Array (LGA)	CC-16-1
ADIS16060/PCBZ <sup>1</sup>		Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

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